Wafer ultra-thinning process for 3D stacked devices and the influences on the device characteristics

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Abstract
In the semiconductor industry, 3D integration using through-silicon via (TSV) has been considered to be a promising way for improving performance and density instead of conventional device scaling. Si wafer thinning is an important technology in 3D stacking. Since the ultra-thin device provides low aspect ratio TSV, several advantages can be expected, such as reduced parasitic RC delay, lower power consumption, and lower TSV residual stress. However, the effects of ultra-thinning on the device are still unclear. In this review, we report the results of the electrical characteristics before and after thinning down to 10 μm using FRAM (Ferroelectric Random Access Memory), HP (High performance) Logic, and DRAM (Dynamic Random Access Memory).

1. INTRODUCTION

Scaling of devices—the driving force of the semiconductor industry—is now facing a major technical and economic transition stage. 3D integration technology using through-silicon via (TSV) has been considered a promising solution to overcome scaling limitations as reported in the example of low volume production using TSV[1]. By connecting stacked chips with the TSV vertical wiring, the wide bandwidth I/O and reduction of interconnects length can be achieved. Further, shorter interconnects lengths lead to the reduction of power consumption as well as parasitic resistance and capacitance. Stacked devices can give us small footprint, and therefore, this technology is expected to be used in mobile devices (Fig. 1)[2]. Si wafer thinning is essential in 3D stacking because multiple devices are stacked. A structure in which ultra-thinned wafers are stacked allows forming a low aspect ratio TSV and reducing parasitic resistance and capacitance. At the same time, lower power consumption, lower TSV residual stress, and lower cost of the TSV process can be achieved (Fig. 2).

However, the effects of ultra-thinning on devices are not well explored yet. In this review, therefore, the effects of thinning on devices will be clarified. To report the thinning limit, electrical characteristics were evaluated and physical analysis was performed using ferroelectric random access memory (FRAM), high performance (HP) logic, and dynamic random access memory (DRAM) wafers thinned to have a Si thickness of 10 μm or less[2-5].

2. WAFER THINNING PROCESS

Si wafers are thinned in two stages: backgrinding (BG) and stress relief (Fig. 3). During the grinding stage, the two types of grinding are performed using wheels with different grit sizes. The grit size is generally described as # (mesh), and the larger the value, the smaller is the grit size. Rough grinding (#320) and fine grinding (#2000) are performed up to their respective specified

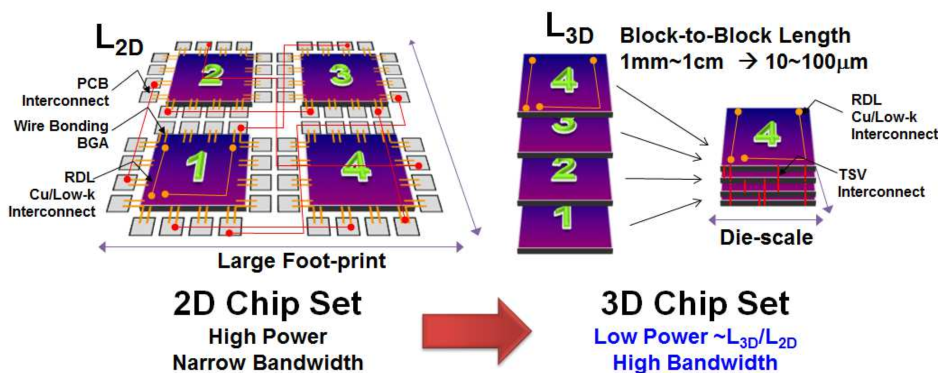

Fig. 1 Comparison between 2D and 3D devices

Advantages of small TSV (or thin wafer)

Performance

- smaller parasitic capacitance
- lower power consumption
- High IO density

Reliability

- lower TSV stress

Cost

- shorter process time

Fig. 2 Advantages of ultra-thinning of Si

thicknesses. In the rough grinding process using a wheel with a large grit size, the grinding speed is high; however, a large damage layer remains on the ground surface. Dislocation and stacking fault can be found at a depth of up to approximately 5 μm. This type of damage layer can be significantly reduced through fine grinding using a wheel with a small grit size. Nevertheless, even after grinding with #2000, a damage layer with the thickness of approximately 0.2 μm remains. When the final Si thickness is sufficiently thick, grinding can be completed with fine grinding. However, because the damage layer at the backside weakens the mechanical strength, stress relief may be required to remove the damage layer in the case of a thin chip. For example, stress relief can be performed using ultra poligrind (UGP), chemical mechanical polish (CMP), and dry polish (DP). The combination of grinding and stress relief is optimized based on the required specifications.

The backside strain and distribution of defects caused by grinding and stress relief were analyzed. The influence of strain caused by thinning was analyzed with μ-Raman spectroscopy. After rough grinding, fine grinding, and CMP, the wafers were measured from the backside in the depth direction using μ-Raman spectroscopy and the strain was calculated from the shift amount (Fig. 4). This graph shows a compressive stress of approximately 450 MPa was generated on the backside after rough grinding and it remained as an elastic stress up to the depth of 40 μm. After fine grinding, the stress near the backside was significantly reduced to 120 MPa, and it remained as an elastic stress up to the depth of 10 μm. After CMP, no residual stress was observed because it was reduced to a level that μ-Raman spectroscopy cannot detect.

The distribution of vacancy-type defects caused by grinding was verified using positron annihilation spectroscopy (Fig. 5). When a positron with a positive charge is captured by a vacancy-type defect after entering a solid, its electron momentum distribution is different from that of the electron at an interstitial site. Therefore, its Doppler broadening is sharpened. When the positron is captured by the vacancy-type defect, the shape parameter (S parameter) becomes larger. In addition, larger the void size, the larger is the S parameter. The distribution of defects simulated from the measurement results of the Si wafer after fine grinding and CMP are shown in Fig. 5. After fine grinding, almost all defects stayed at a depth of approximately 100 nm from the backside, which is identical to the TEM observation results. After the CMP, in accordance with the removal of the damage layer, defects are slightly distributed up to the depth of 10 nm from the backside.

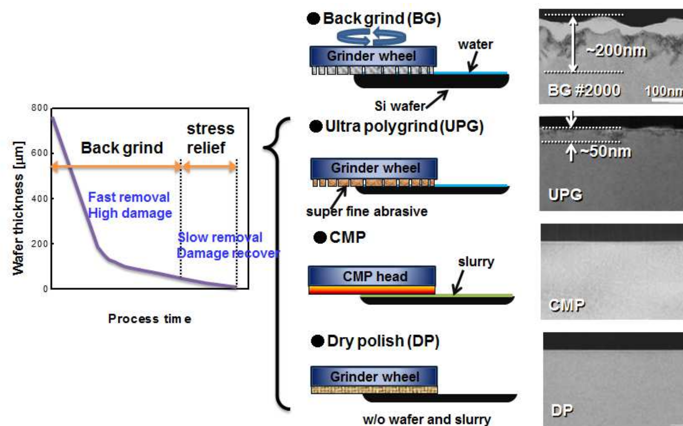

Fig. 3 Si wafer thinning process and backside TEM images after grinding and stress relief

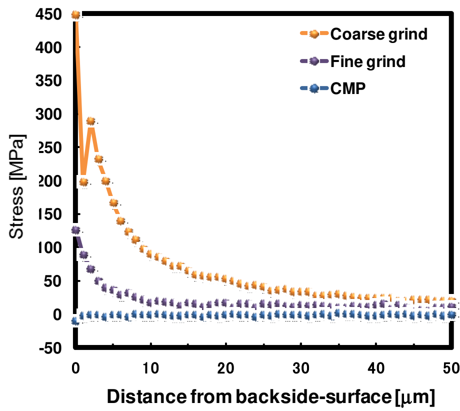

Fig. 4 Depth profile of strain distribution using µ-Raman spectroscopy (calculated from shift amount)

As shown above, depending on the thinning process, the backside strain and defect distribution are significantly changed. Hereinafter, influences of these strains and defects on devices will be verified.

3. EXPERIMENTAL

Device wafer thinning and evaluation flow using the wafer-on-a-wafer (WOW) process is introduced in this section (Fig. 6)[6]. The effects of thinning were evaluated using 180-nm node FRAM, 45-nm node HP logic, and 40-nm node DRAM wafers.

After the device side of the wafer is bonded to the first support substrate where the temporary bond

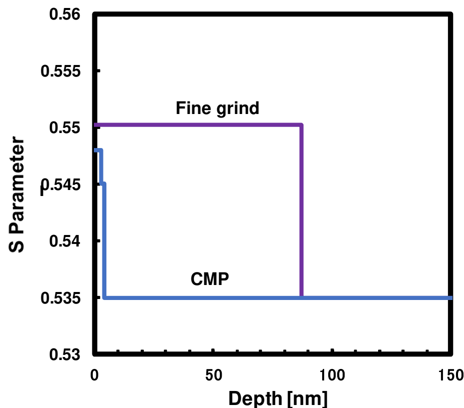

Fig. 5 Distribution of defects simulated from the measurement results of positron annihilation spectroscopy

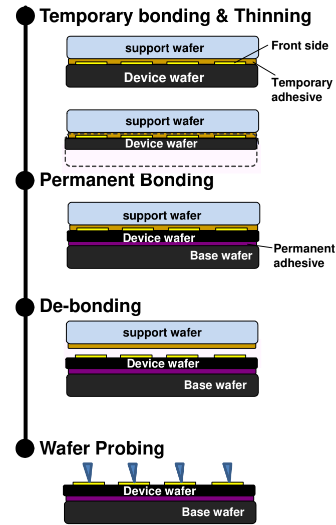

Fig. 6 Device wafer thinning and evaluation flow using WOW process

is coated, the wafer is thinned to the target thickness by grinding. For the thinning process, only the stress relief method is varied depending on the device type. The target remaining Si thickness was 4-40 µm (Table 1). The Grinder/Polisher DGP8761 (DISCO) was used for grinding. Total thickness variation (TTV) was less than 2 µm within a 300 mm wafer after thinning. The thinned device wafer was mounted on the second support substrate where the permanent bond is coated, and the electrical characteristics were evaluated after de-bonding the first support substrate.

Table 1 Wafer thinning process and target Si thickness for each device type

Device	Coarse grind	Fine grind	stress relief	Final Si thickness [µm]
FRAM	#320	#2000	CMP	9
HP Logic	#320	#2000	UPG	7
DRAM	#320	#2000	w/o	40~4

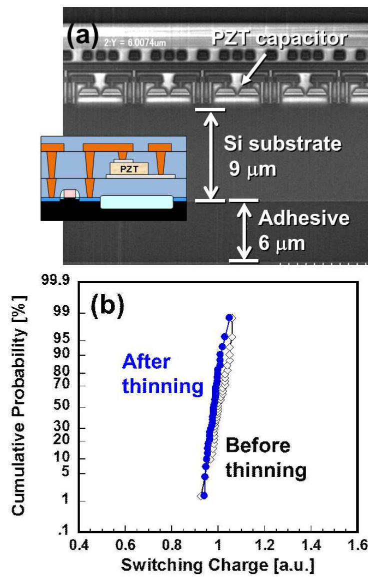

Fig. 7 (a) A SEM cross-sectional image of the FRAM wafer after thinning and (b) hysteresis property before and after thinning.

4. RESULTS AND DISCUSSION

The characteristics before and after the thinning of FRAM, which is used as non-volatile memory, were examined. FRAM uses ferroelectrics as a capacitor. If hydrogen is incorporated in the ferroelectric film, it deprives oxygen from the ferroelectric crystals. This causes a defect, and therefore, the polarization characteristic of the ferroelectric film is degraded. In order to verify the influence of moisture, the CMP process was

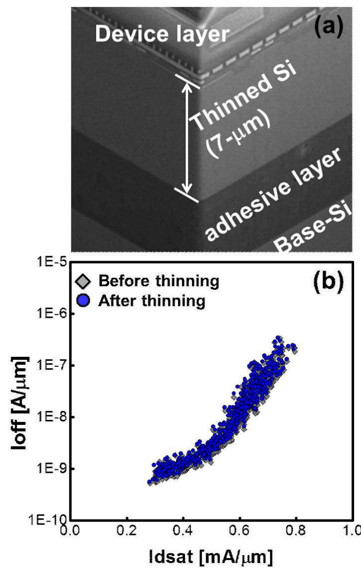

Fig. 8 (a) A SEM cross-sectional image of the HP logic wafer after thinning and (b) drive electrical characteristics before and after thinning

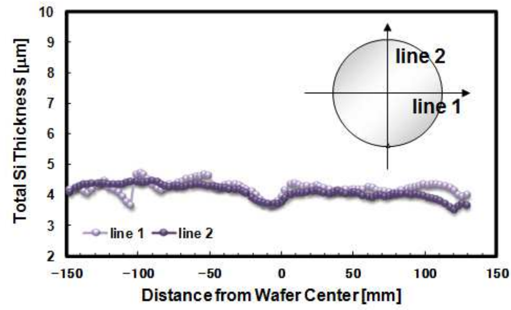

Fig. 9 TTV measurement results of the DRAM wafer thinned to 4 μm

applied as stress relief process. Fig. 7 shows the SEM cross-sectional image and hysteresis property of the FRAM wafer thinned up to a thickness of 9 μm. Because the hysteresis property before and after thinning shows only the difference within the measurement error scope, it indicates that the thinning and wet processes did not cause degradation.

Next, the influence of thinning on the HP logic device will be explained. The HP logic wafer was processed with UPG as stress relief from the mechanical strength and gettering property aspect to thin it to have the remaining Si thickness of 7 μm. For this logic wafer, strain technology was introduced to enhance the transistor performance by improving electron mobility. This type of wafer also has a Cu/Low-k interconnects structure to improve RC delay, and its mechanical strength

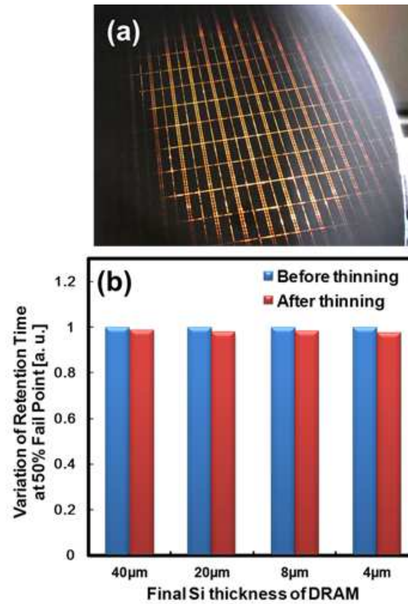

Fig. 10 (a) An image of the DRAM wafer thinned to 4 μm and (b) the retention property before and after thinning.

is weaker than that of the Al/SiO_2 interconnects. That is, it seems to be easily influenced by the residual stress on the backside and the thinning process. However, even when the wafer was thinned to have a remaining Si thickness of 7 µm, the transistor drive current did not change (Fig. 8). This result indicates that residual stress and defects that occur after UPG do not affect the characteristics of logic devices.

Finally, the effect of the remaining Si thickness on device characteristics was thoroughly examined using the DRAM wafer. The Si thickness was in the range from 4-40 µm and only rough grinding and fine grinding were performed. TTV ranged from 1.02 to 1.94 µm when a 300 mm wafer was processed. When the thickness was 4 µm, TTV of 1.02 µm could be obtained (Fig. 9). The thickness of 4 µm is equivalent to 0.5 % of the original thickness (775 µm) and it is sufficiently thin for visible light to penetrate (Fig. 10 (a)). The variations of the retention characteristic for the Si remaining thickness were examined, but even when the wafer was thinned to 4 µm, no degradation was observed (Fig. 10 (b)). As explained in Chapter 2, compressive stress and defects remain at the backside, and the retention characteristic does not change after thinning. Therefore, it can be explained that stress and defects caused by grinding do not affect thicknesses up to 4 µm.

5. CONCLUSION

The variations of electrical characteristics when the FRAM, HP logic, and DRAM wafers were ultra-thinned using the WOW technology were examined. With this technology, the variations of Si thickness could be 2 µm or less. In order to clarify the thinning effects on devices, the thinning of FRAM, HP logic, and DRAM wafers with Si thicknesses of 9, 7, and 4 µm, respectively, were evaluated. However, the degradation of these device wafers was not observed. In addition, the physical analysis results did not reveal the effects of strain and defects caused by thinning.

The use of ultra-thin Si devices substantially shortens the interconnects length of a stacked chip and greatly reduces parasitic resistance and capacitance compared with conventional devices. We are working on further optimization and development of our technologies aiming at providing ultra-thin devices.

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